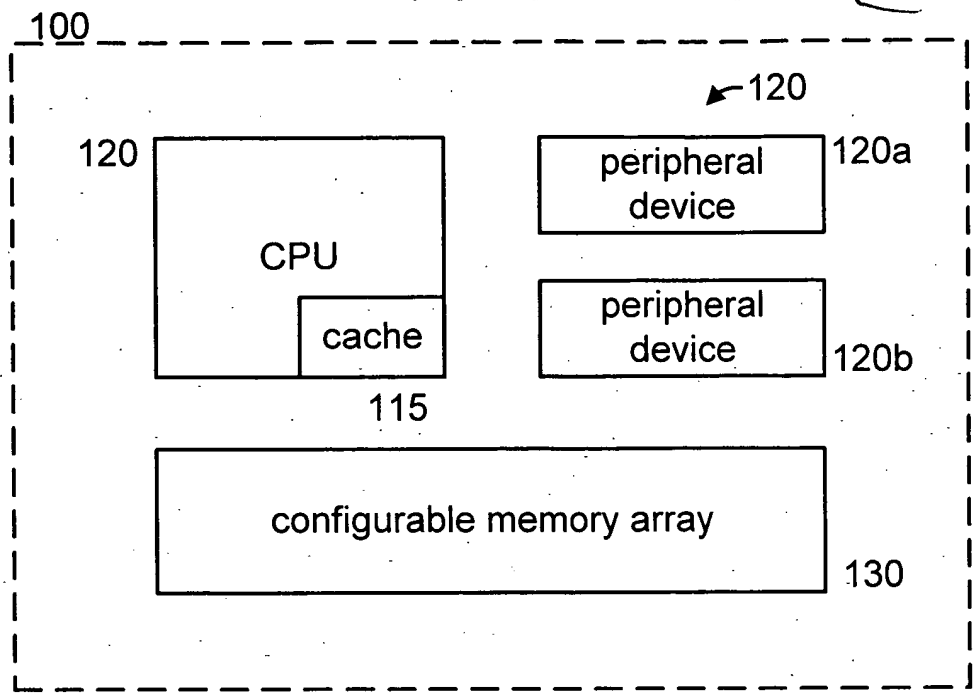

FIG. 1

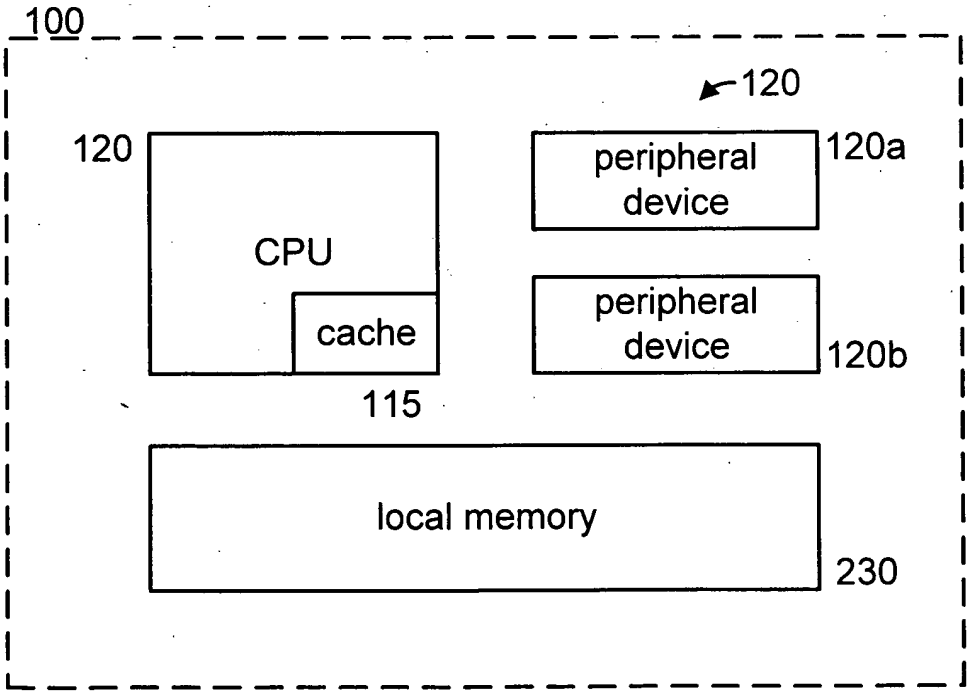

FIG. 2

YOR9-2001-0602 (8728-546)

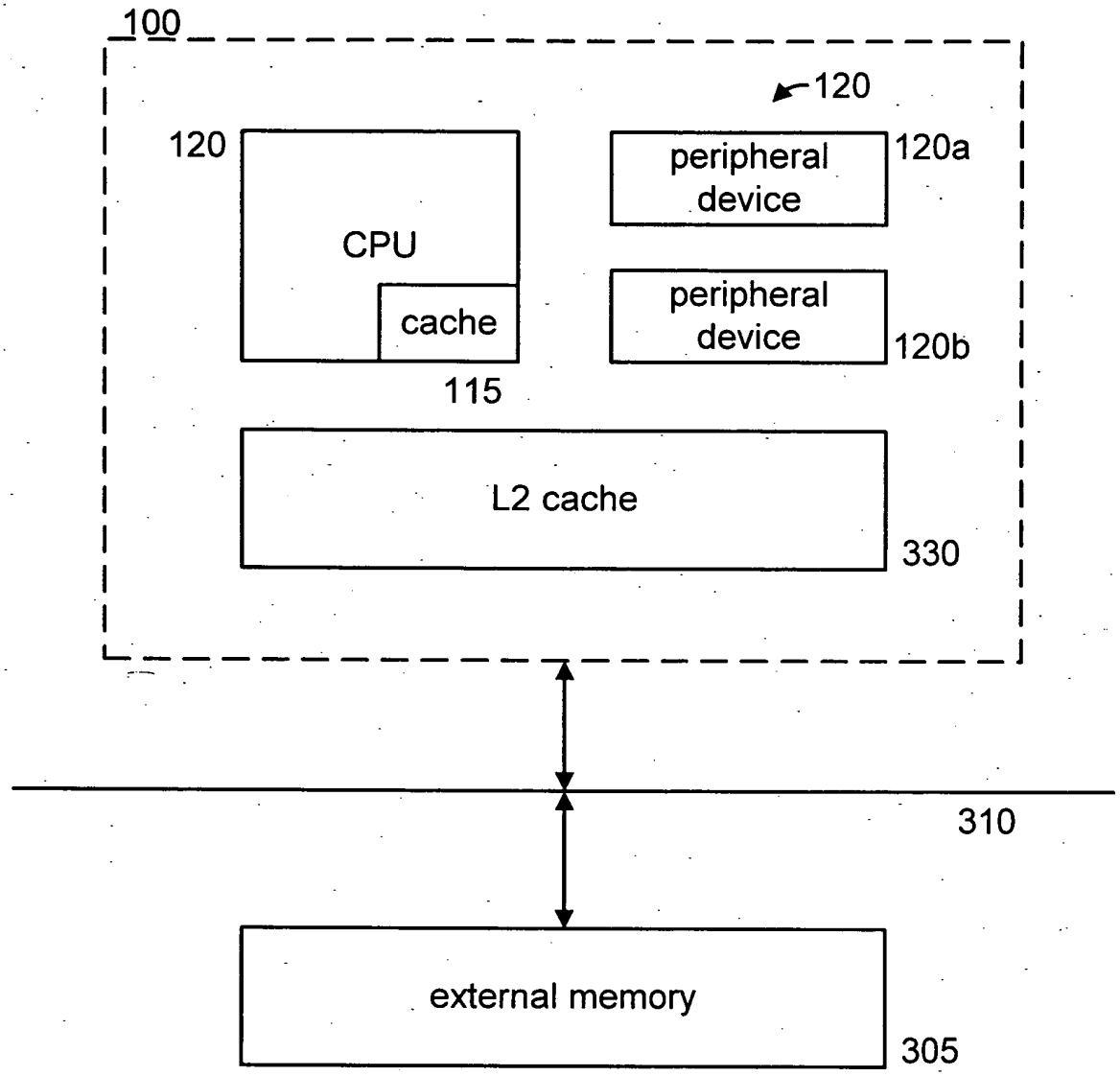

FIG. 3

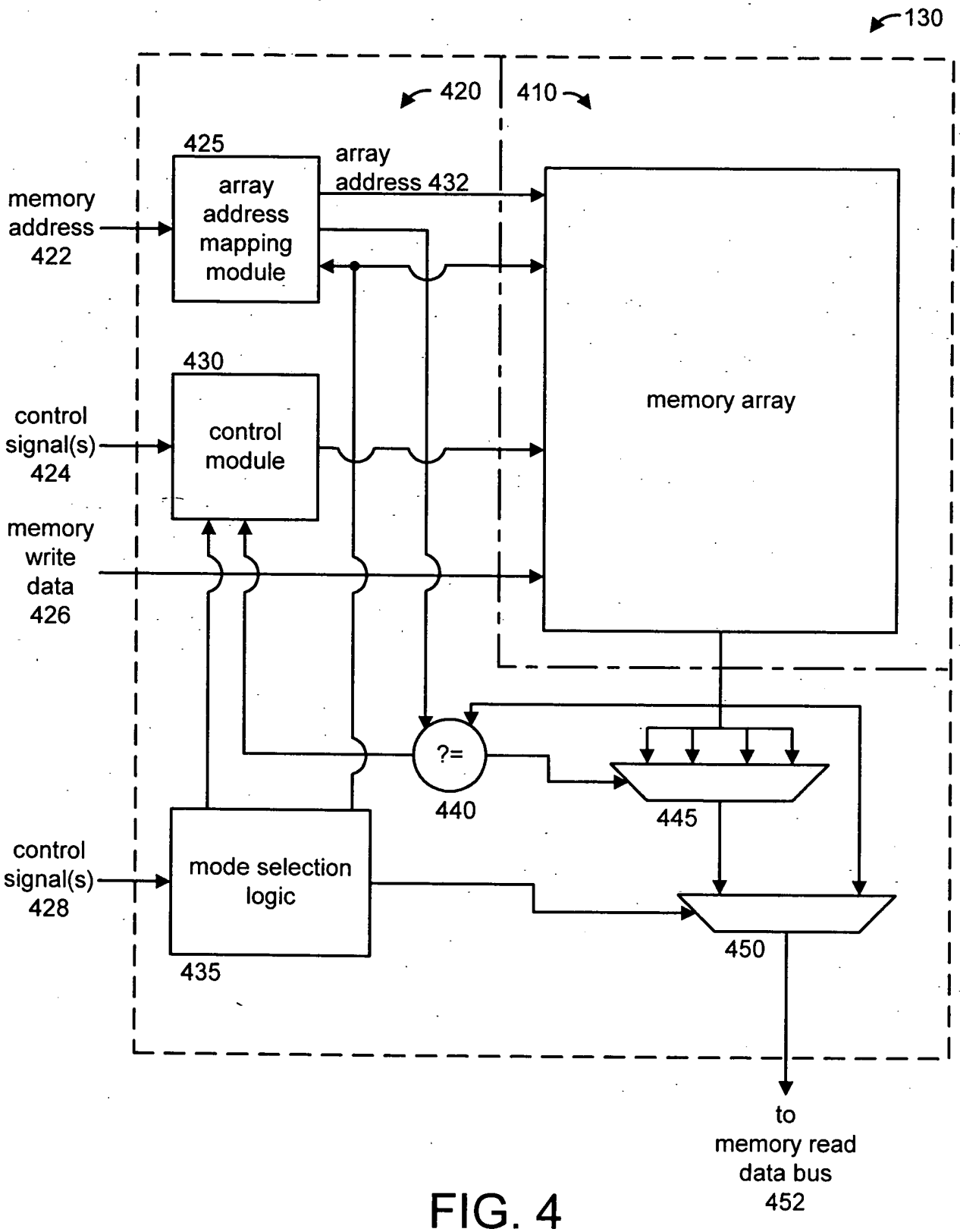
130
420
410
425
array address mapping module
array address 432
memory address 422
430
control module
control signal(s) 424
memory write data 426
memory array
?=
440
445
control signal(s) 428
mode selection logic
435
450
to memory read data bus 452

FIG. 4

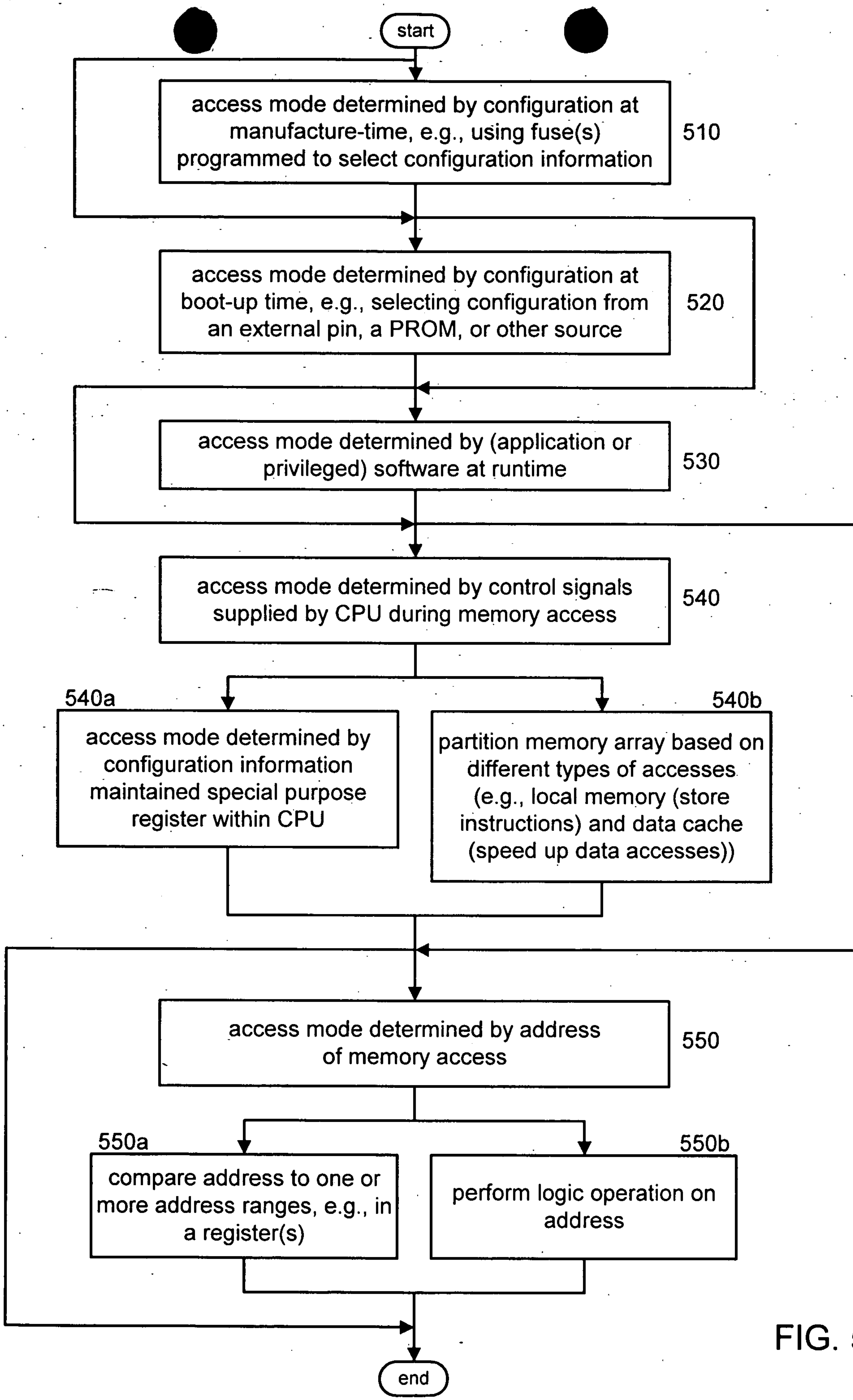
start
access mode determined by configuration at manufacture-time, e.g., using fuse(s) programmed to select configuration information
510
access mode determined by configuration at boot-up time, e.g., selecting configuration from an external pin, a PROM, or other source
520
access mode determined by (application or privileged) software at runtime
530
access mode determined by control signals supplied by CPU during memory access
540
540a
access mode determined by configuration information maintained special purpose register within CPU
540b
partition memory array based on different types of accesses (e.g., local memory (store instructions) and data cache (speed up data accesses))
access mode determined by address of memory access
550
550a
compare address to one or more address ranges, e.g., in a register(s)
550b
perform logic operation on address
end

FIG. 5

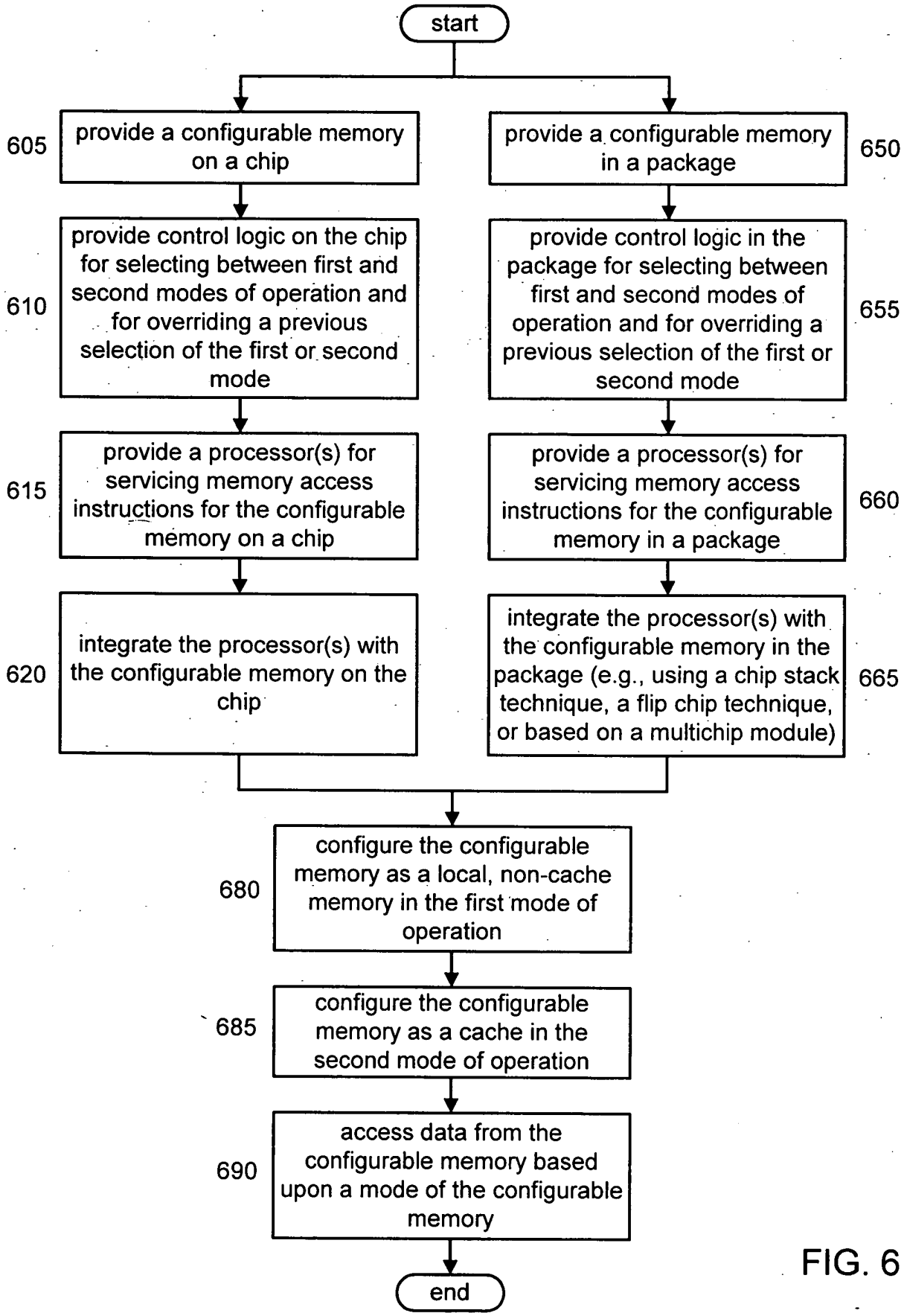

FIG. 6